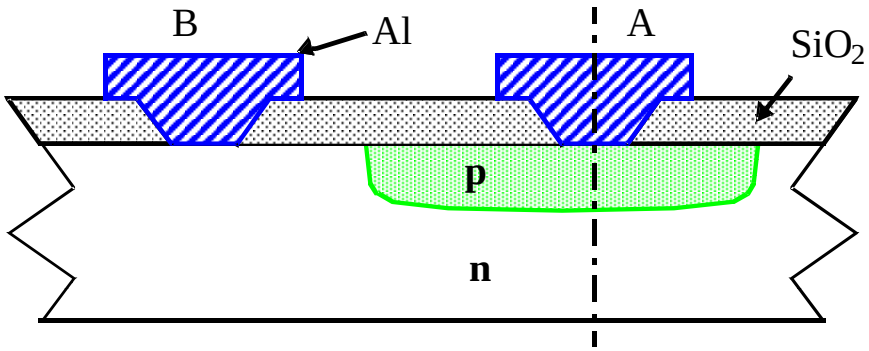
ECE680: Physical VLSI Design

Chapter III

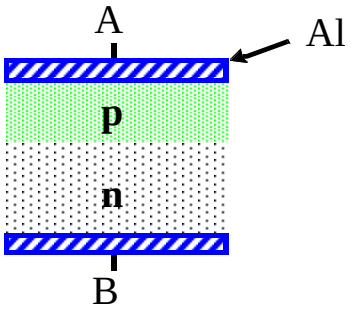
CMOS Device, Inverter, Combinational circuit Logic and Layout

Part 1 The MOS Transistor

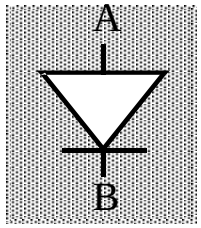
The Diode



Cross-section of pn-junction in an IC process

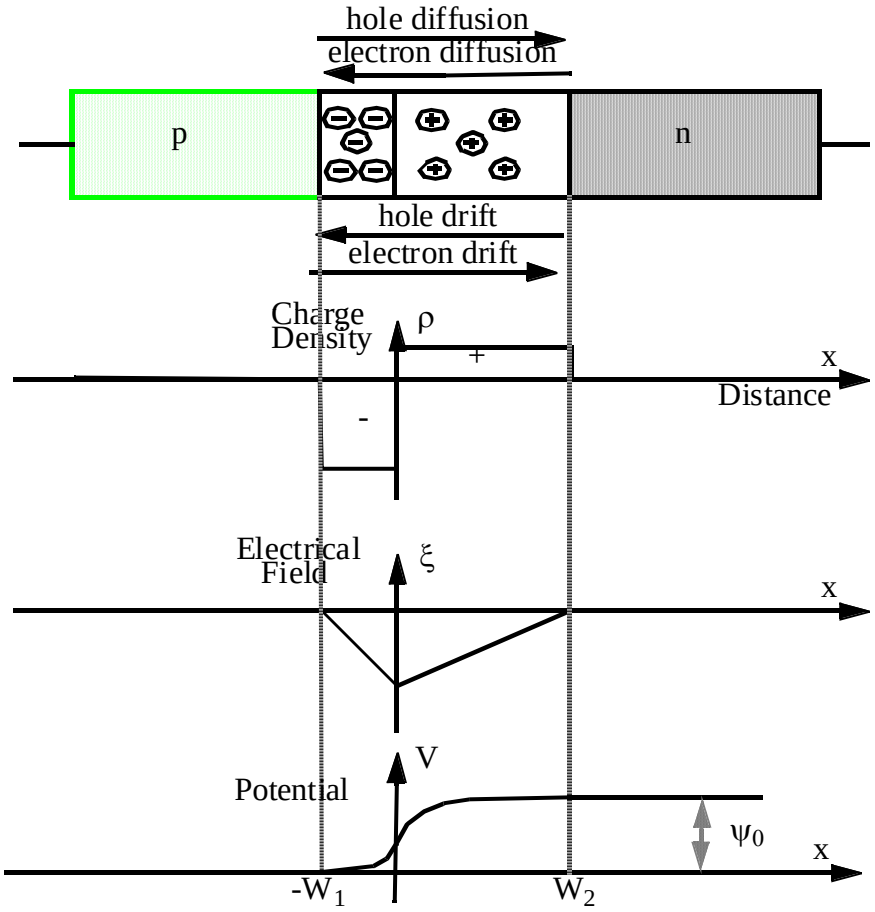


One-dimensional representation



diode symbol

Depletion Region



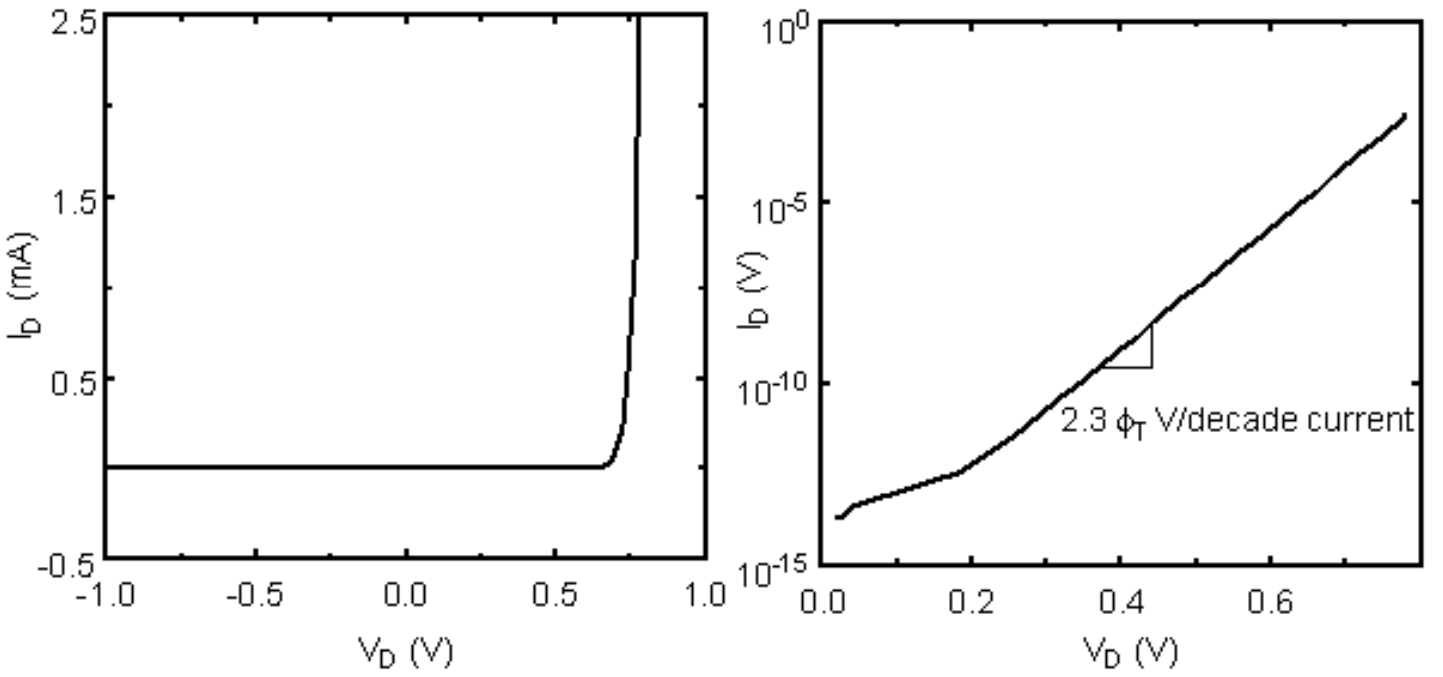
(a) Current flow.

(b) Charge density.

(c) Electric field.

(d) Electrostatic potential.

Diode Current

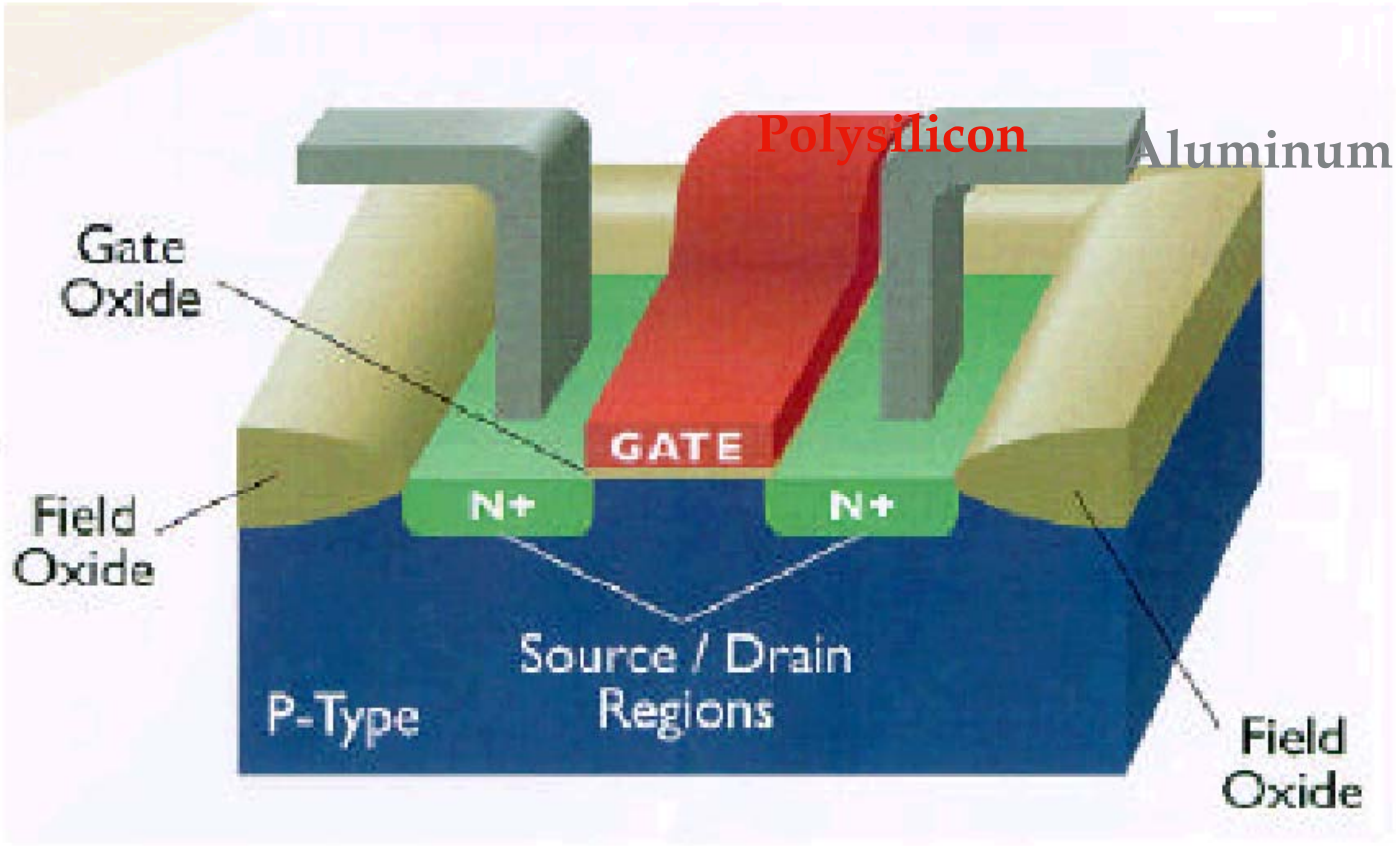


(a) On a linear scale.

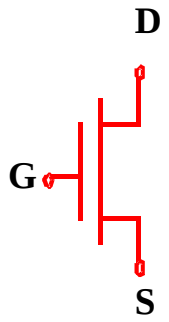
(b) On a logarithmic scale (forward bias).

$$I_D = I_S\left(e^{V_D/\phi_T} - 1\right)$$

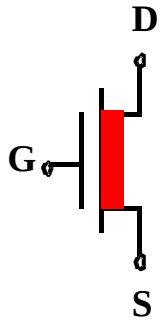
The MOS Transistor



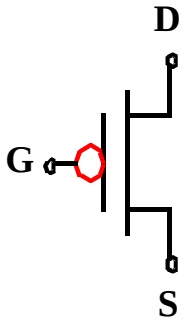
MOS Transistors: Types and Symbols



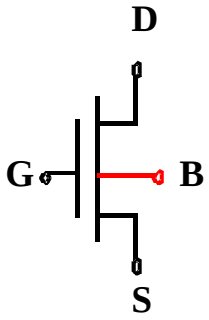
NMOS Enhancement



NMOS Depletion

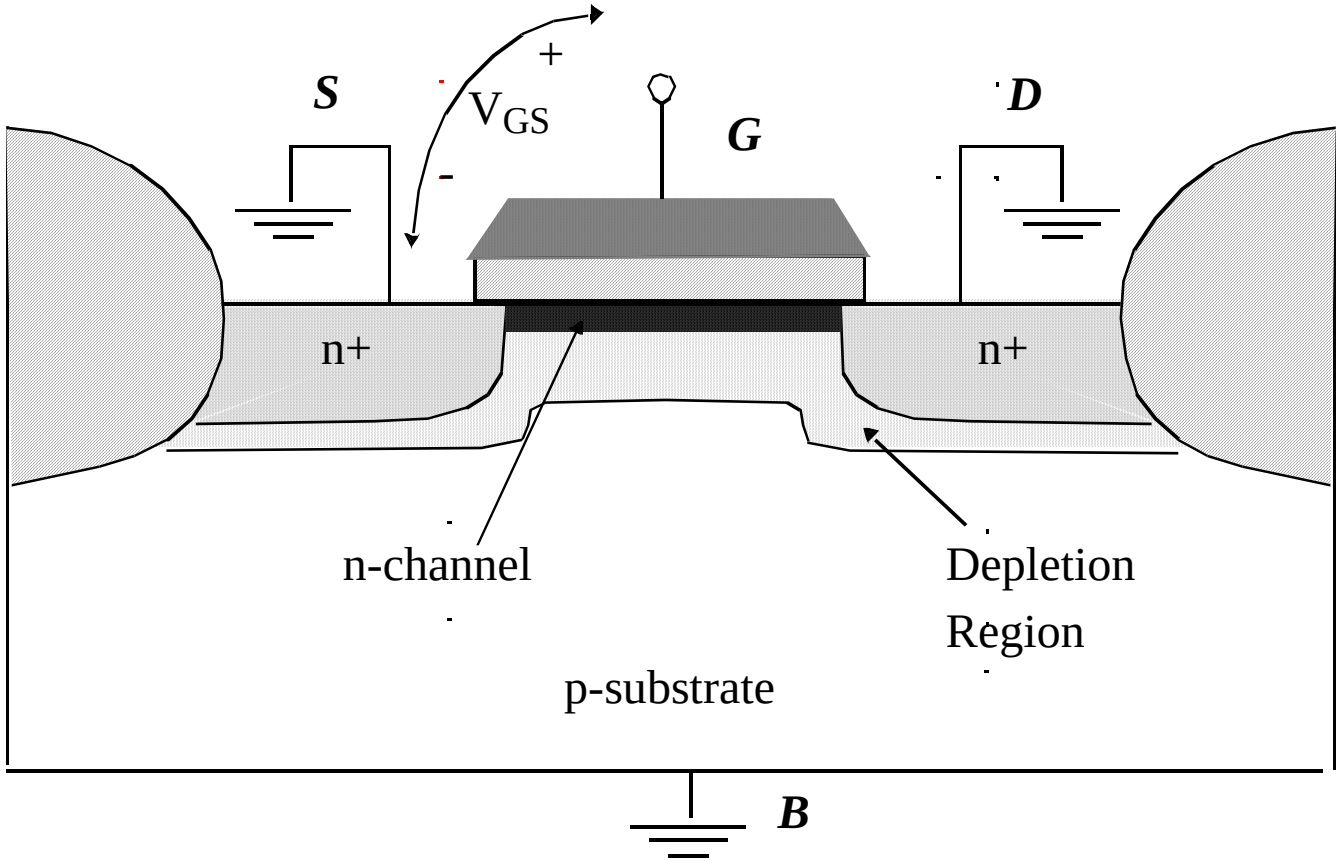


PMOS Enhancement



NMOS with Bulk Contact

Threshold Voltage: Concept



The Threshold Voltage

$$V_T = \phi_{ms} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

Workfunction Difference

Depletion Layer Charge

Surface Charge

Implants

Body Effect Coefficient

$$V_T = V_{T0} + \gamma\left(\sqrt{\left|-2\phi_F + V_{SB}\right|} - \sqrt{\left|-2\phi_F\right|}\right)$$

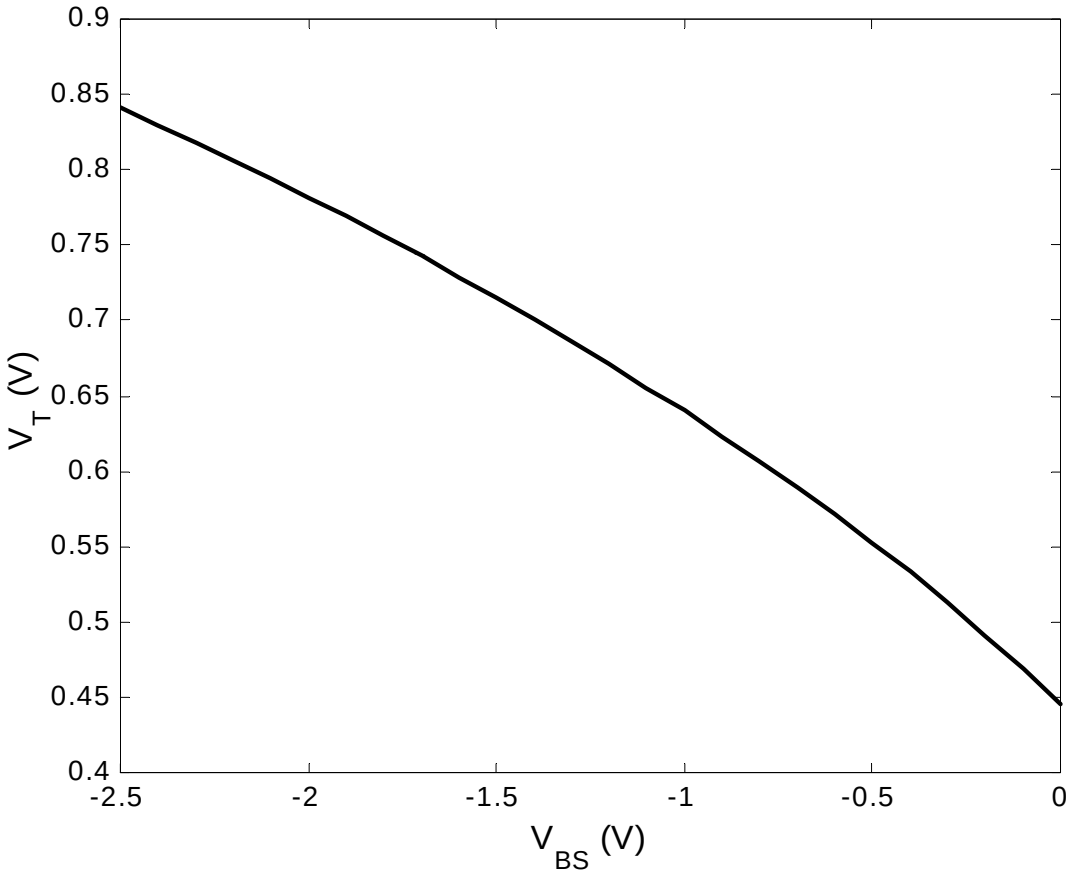
with

$$V_{T0} = \phi_{ms} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

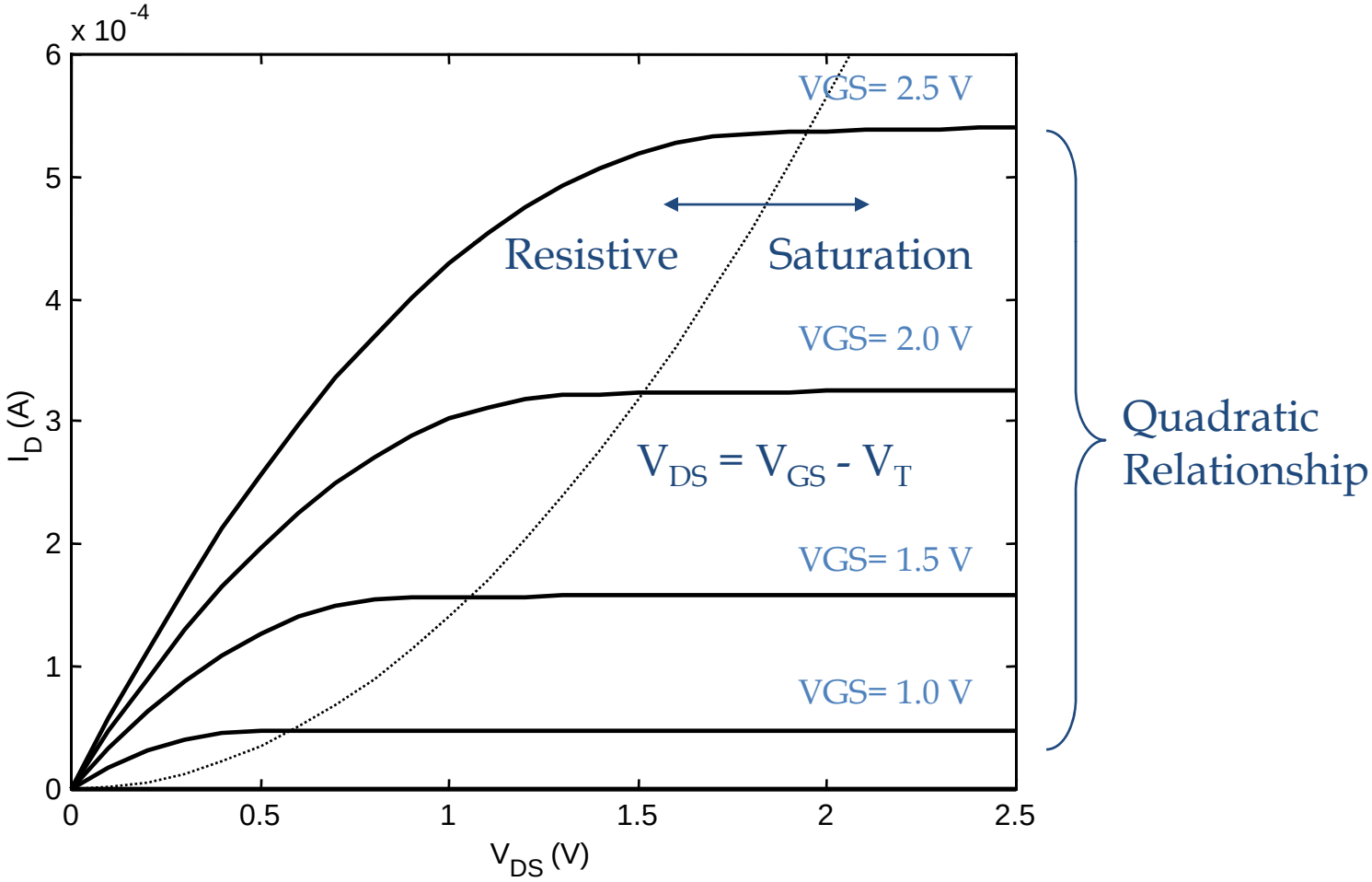
and

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

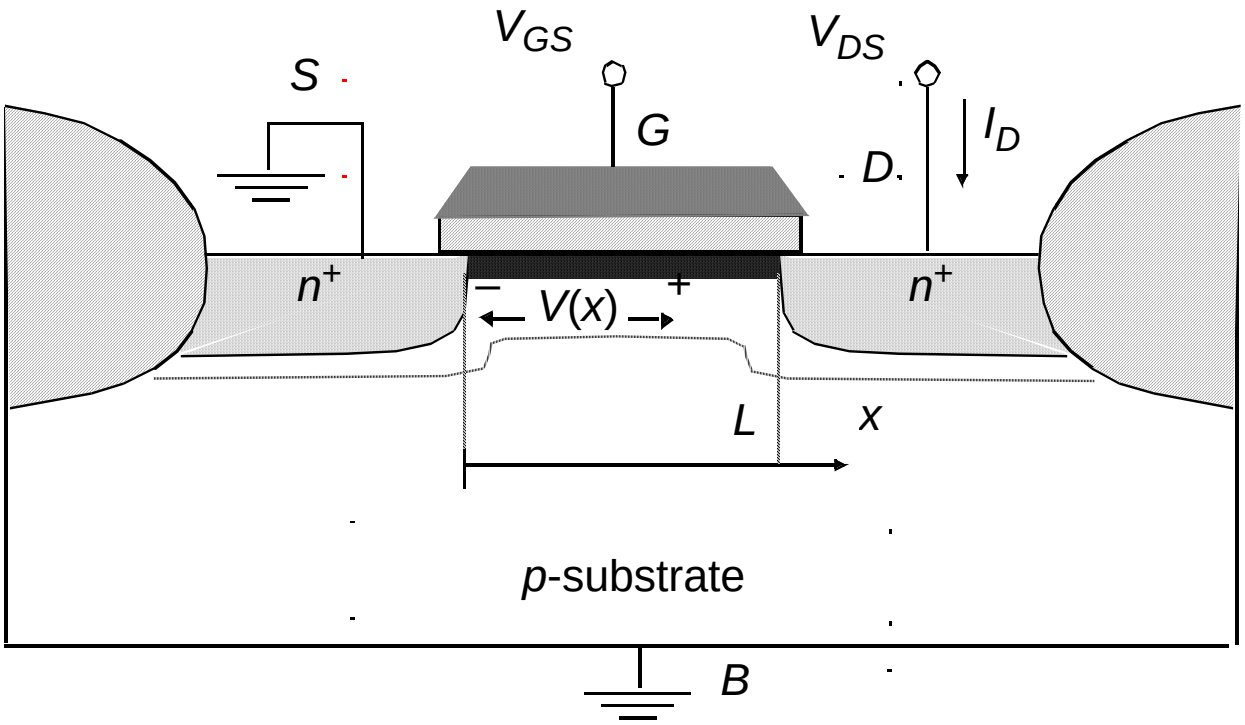
The Body Effect



Standard NMOS I-V Curves

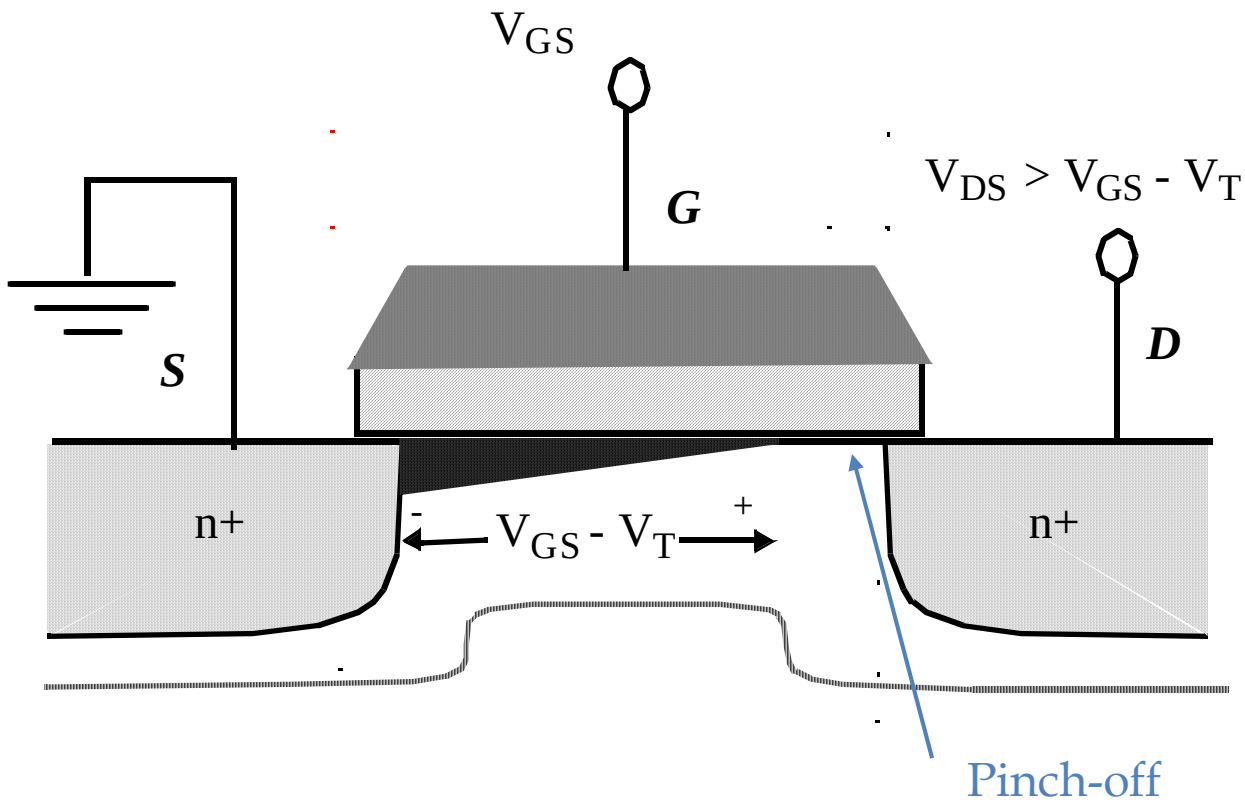


Transistor in Linear



MOS transistor and its bias conditions

Transistor in Saturation



Long-Channel I-V Model

Linear Region: $V_{DS} \leq V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$$

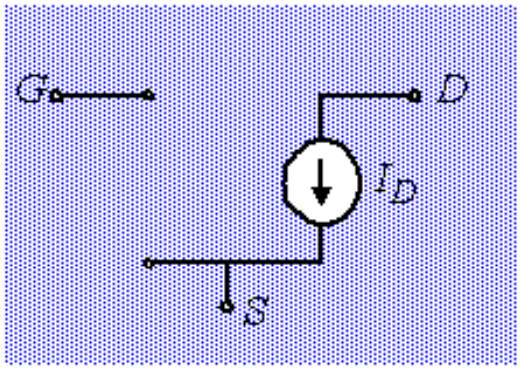
Process Transconductance Parameter

Saturation Mode: $V_{DS} \geq V_{GS} - V_T$

Channel Length Modulation

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

A model for manual analysis



$$V_{DS} > V_{GS} - V_T$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

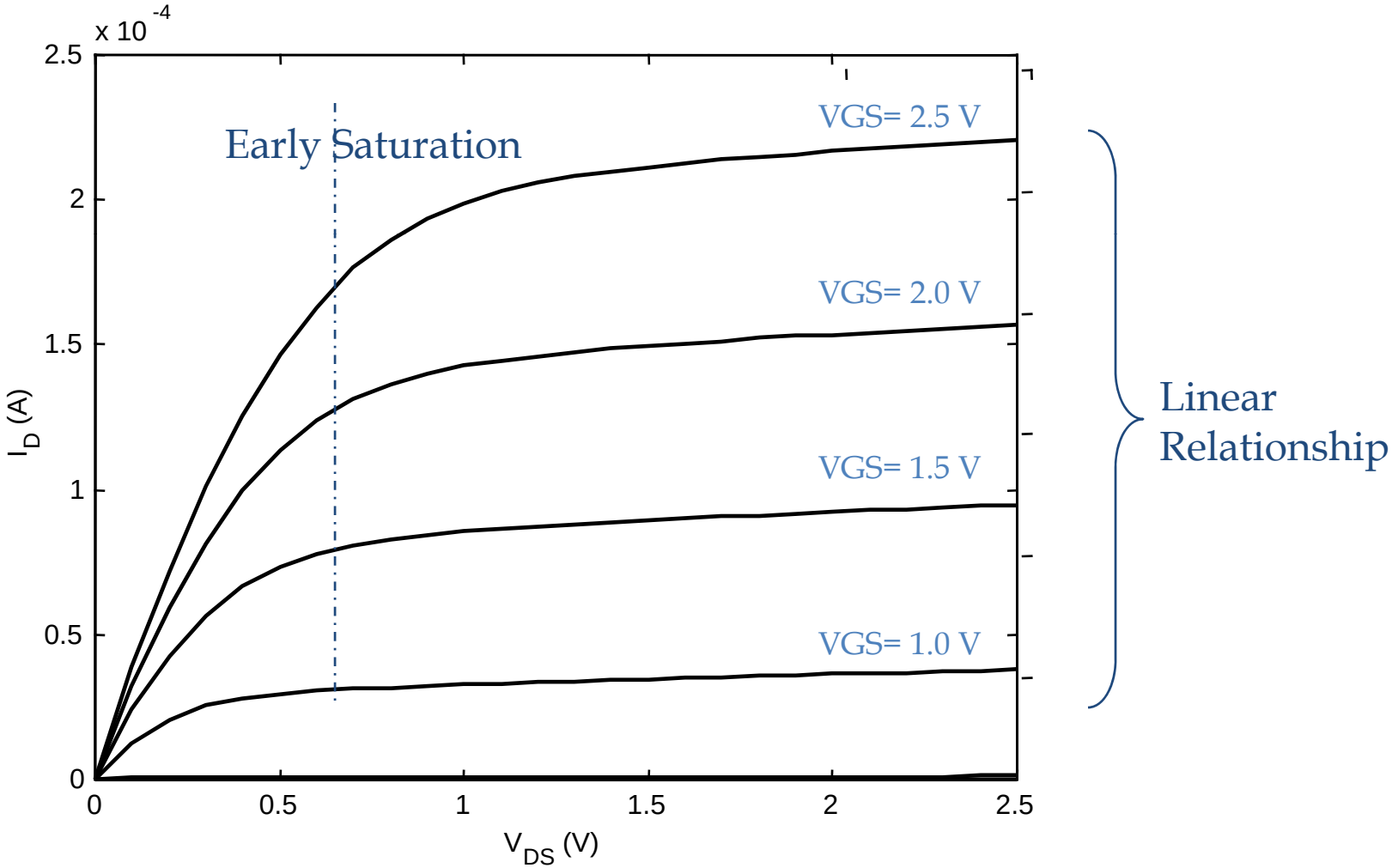
$$V_{DS} < V_{GS} - V_T$$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

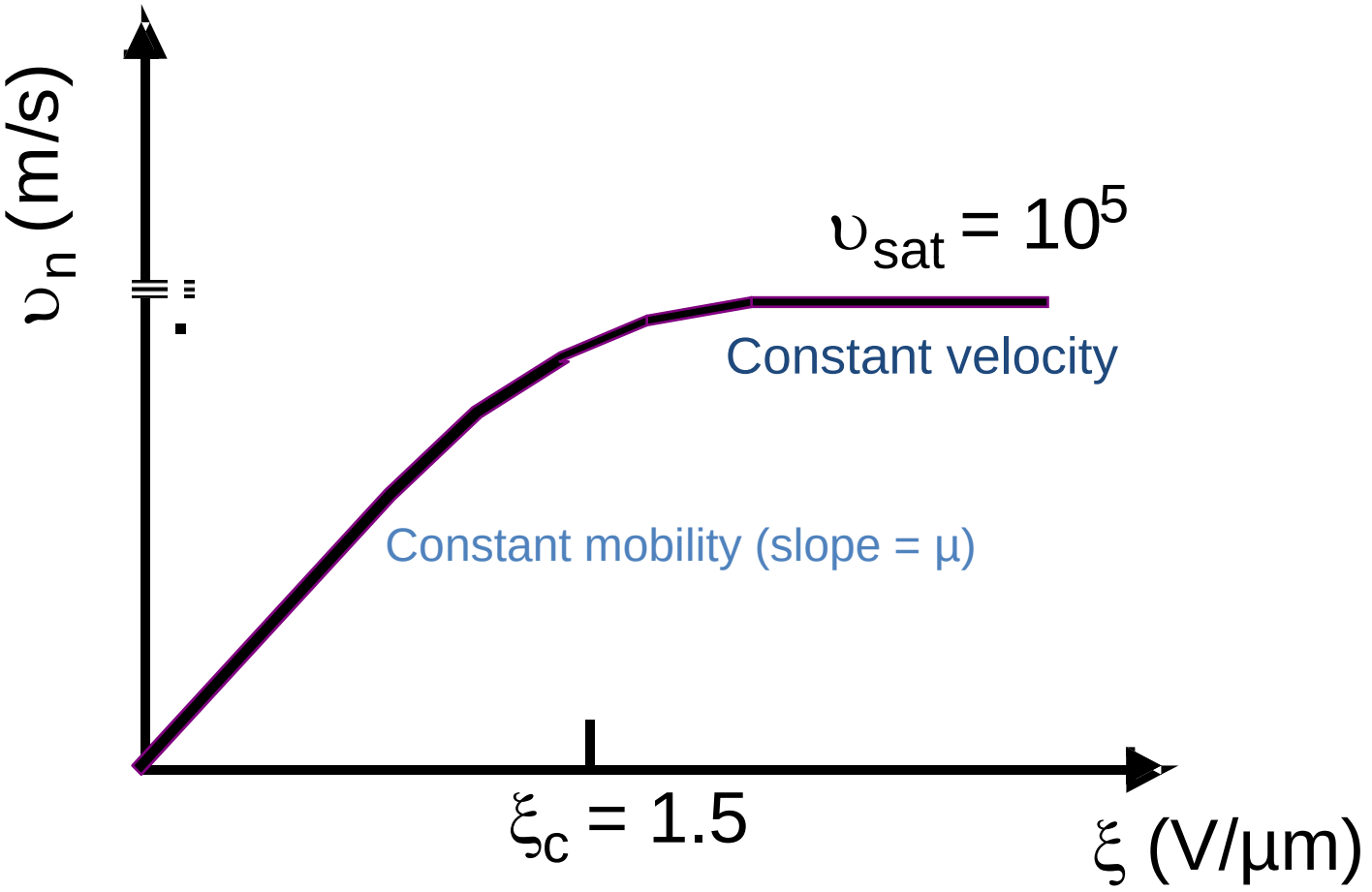
with

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

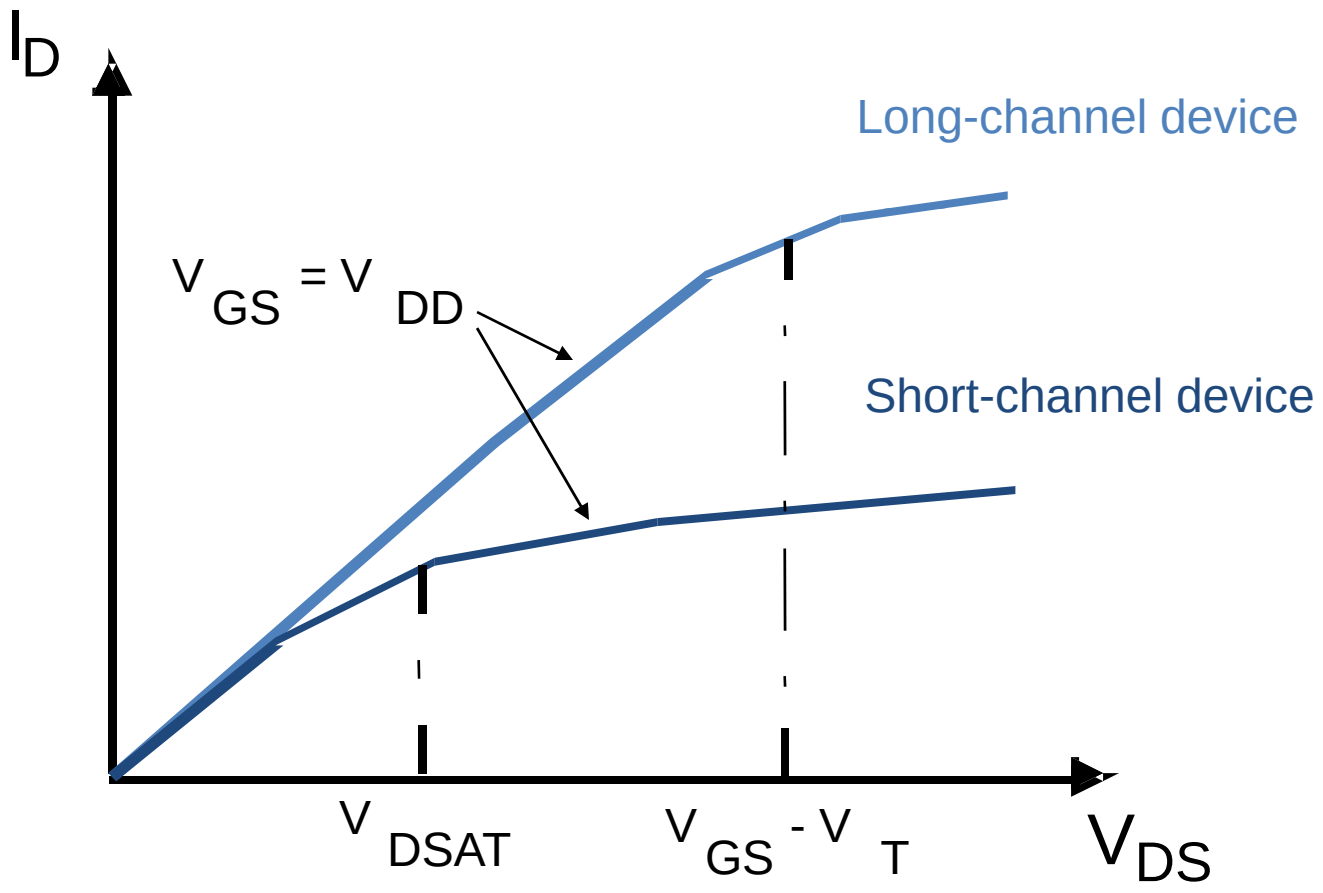
Deep-Submicron I-V Model



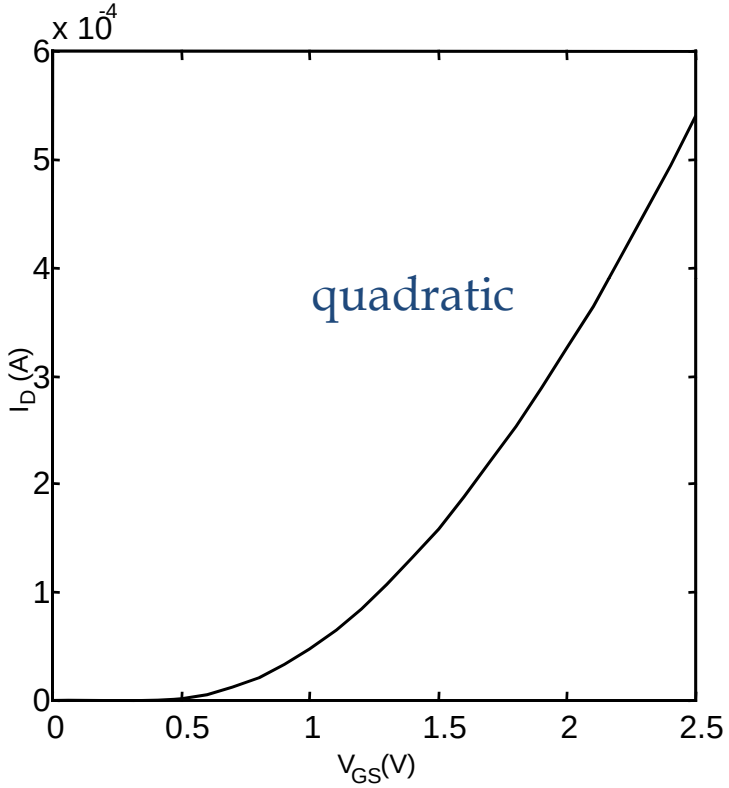
Velocity Saturation



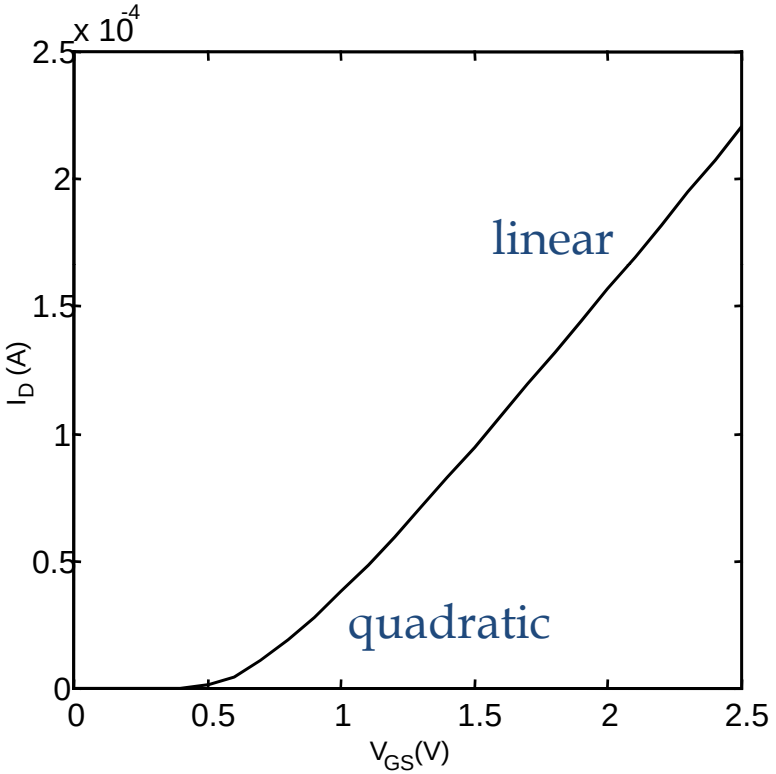
Short-Channel I-V Model



I_D versus V_{GS}

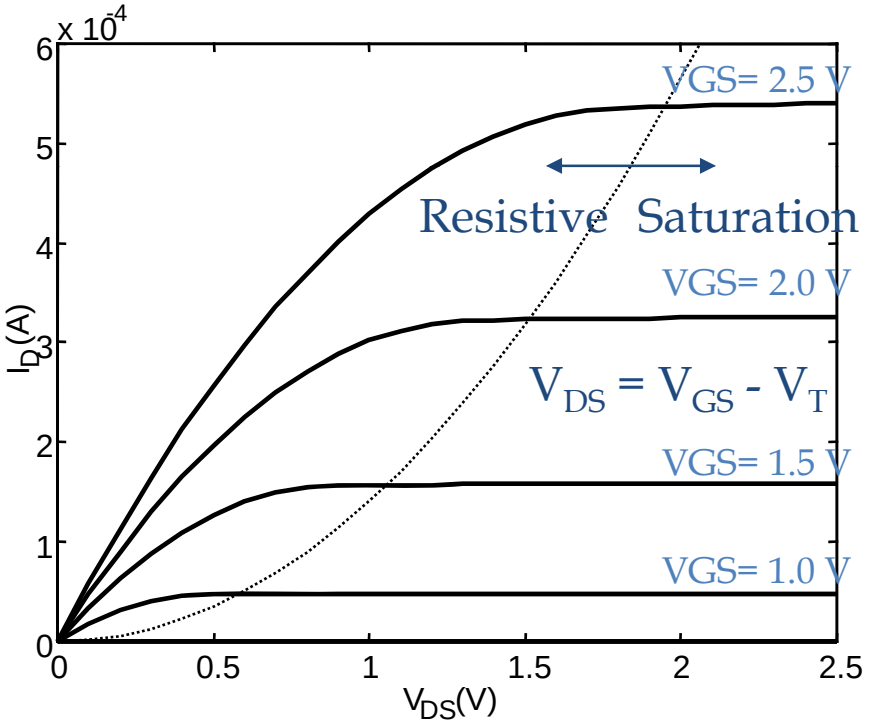


Long Channel

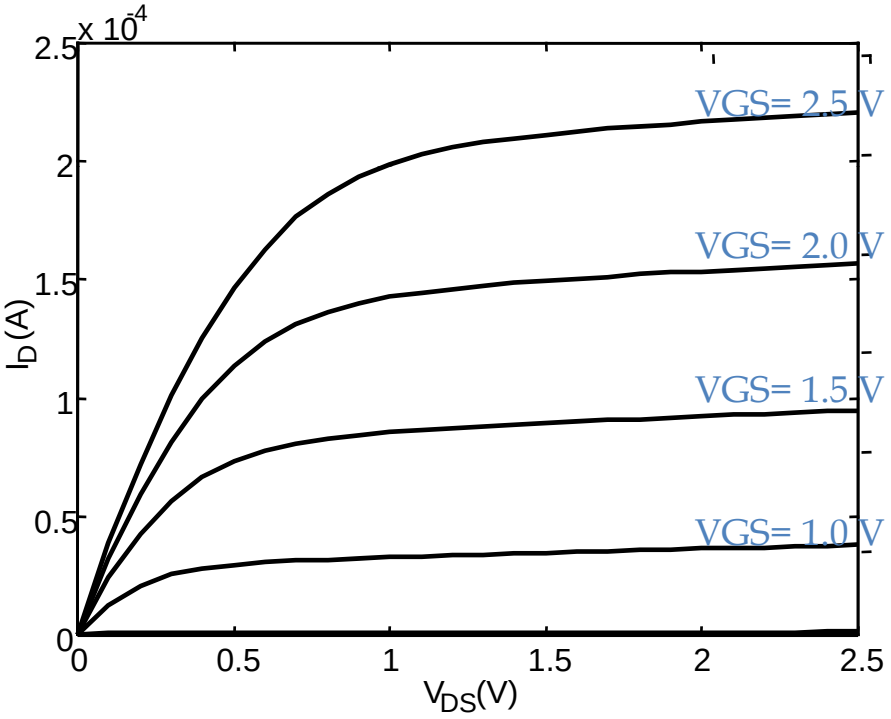


Short Channel

I_D versus V_{DS}



Long Channel



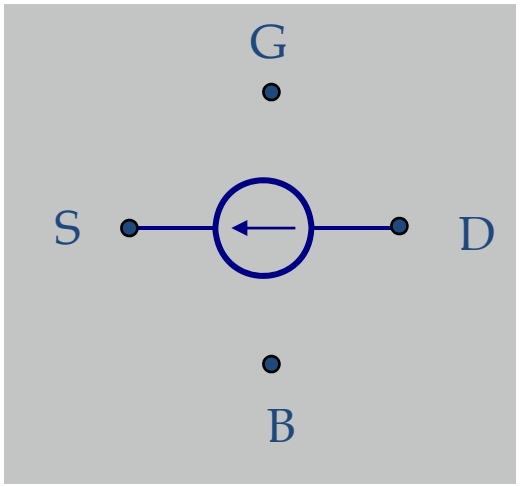
Short Channel

Simplified Model for Velocity Saturation

- Assume abrubt transition from saturation to velocity saturation.
- Assume V_{DS} term ≈ $L\xi_C$ (constant throughout Velocity Saturation Region)
  Call this Value V_{DSAT}
- New equation:

$$I_D = k' \frac{W}{L} \left[(V_{GS} - V_T) V_{DSAT} - \frac{V_{DSAT}^2}{2} \right] (1 + \lambda \quad V_{DS})$$

A Unified Model: for Manual Analysis



$$I_D = 0 \quad \text{for} \quad V_{GT} \le 0$$

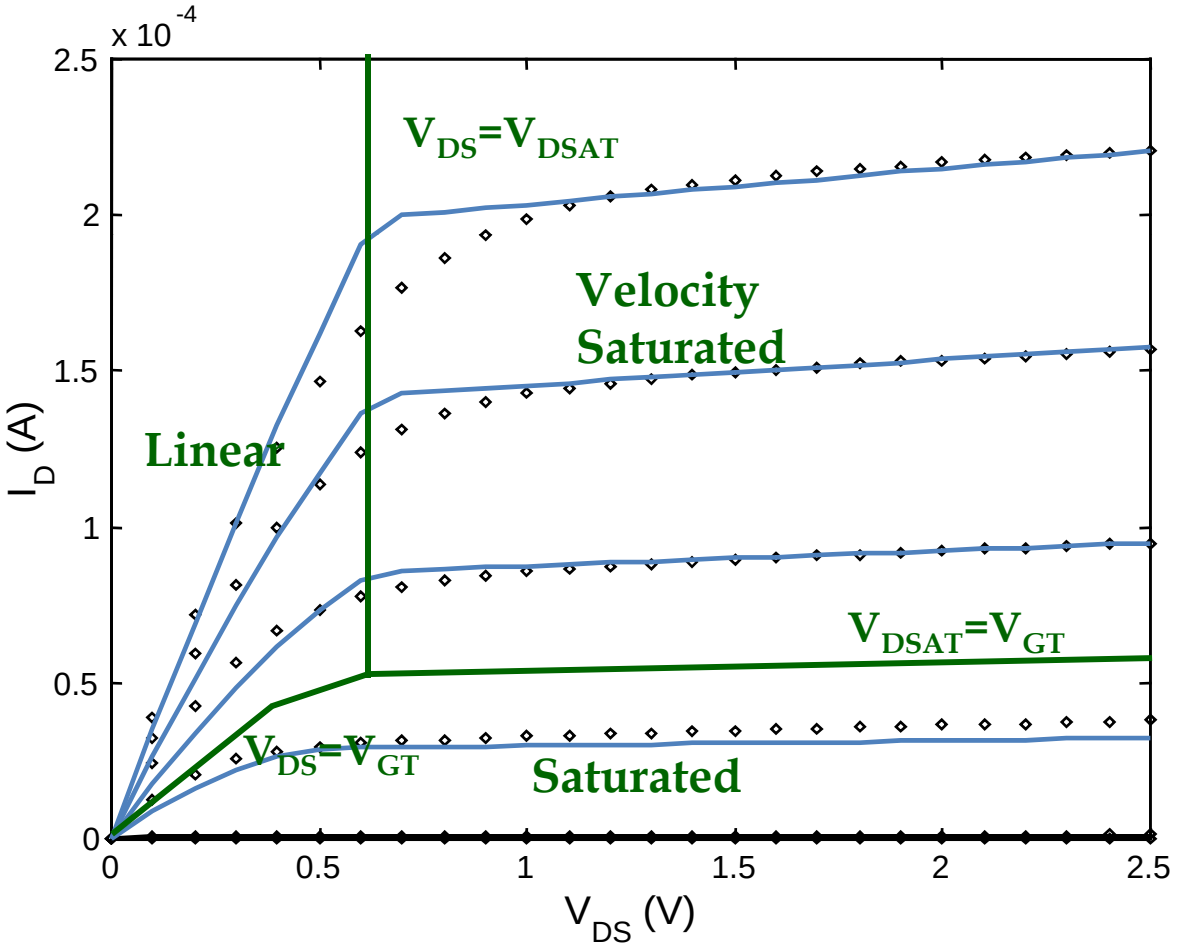
$$I_D = k' \frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \text{ for } V_{GT} \ge 0$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$,

$V_{GT} = V_{GS} - V_T$,

and $V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$

Simple Model versus SPICE



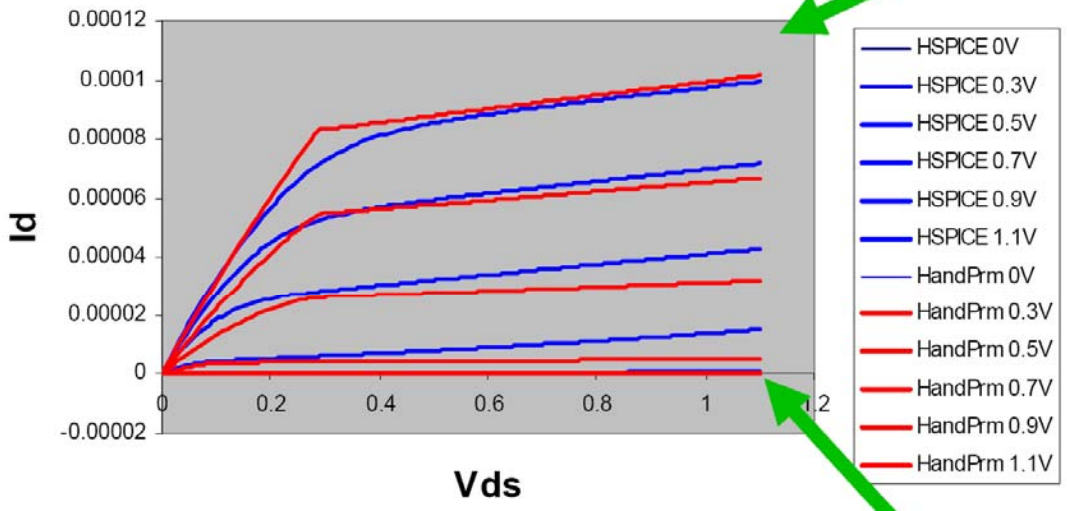
Transistor Model: for Manual Analysis

Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

	V_{T0} (V)	γ ($V^{0.5}$)	V_{DSAT} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	−0.4	-0.4	-1	-30×10^{-6}	-0.1

	C_{ox} ($fF/\mu m^2$)	C_O ($fF/\mu m$)	C_j ($fF/\mu m^2$)	m_j	ϕ_b (V)	C_{jsw} ($fF/\mu m$)	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

Problem: Low Output Resistance



Vgs = 1.1V
Good Match!

Vgs = 0.5V
Model doesn't capture the low output resistance

Modified Unified Model

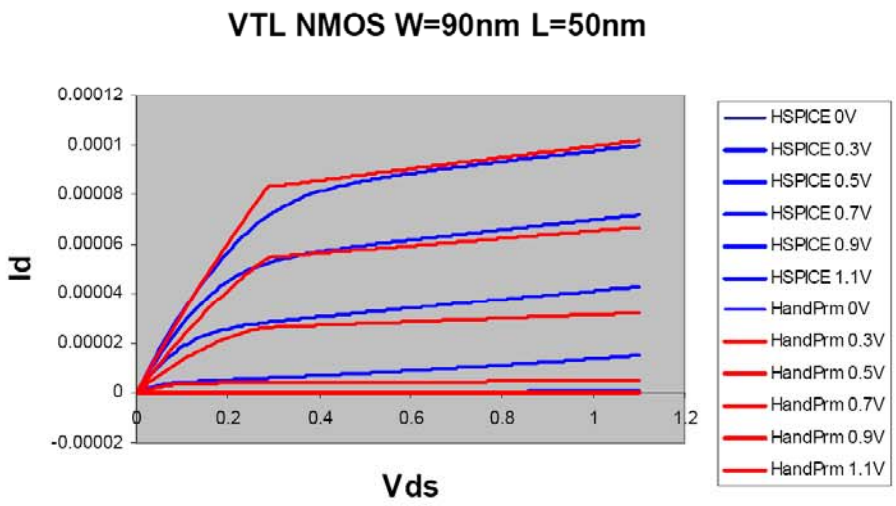
$$I_D = 0 \quad \text{when} \quad (V_{GS} - V_T) \le 0$$

$$I_D = k' \frac{W}{L}\left[(V_{GS} - V_T)V_{\min} - \frac{V_{\min}^{\ 2}}{2}\right](1 + \lambda \quad V_{DS}) + \frac{V_{DS}W}{r_{ch}} \quad \text{when} \quad (V_{GS} - V_T) > 0$$

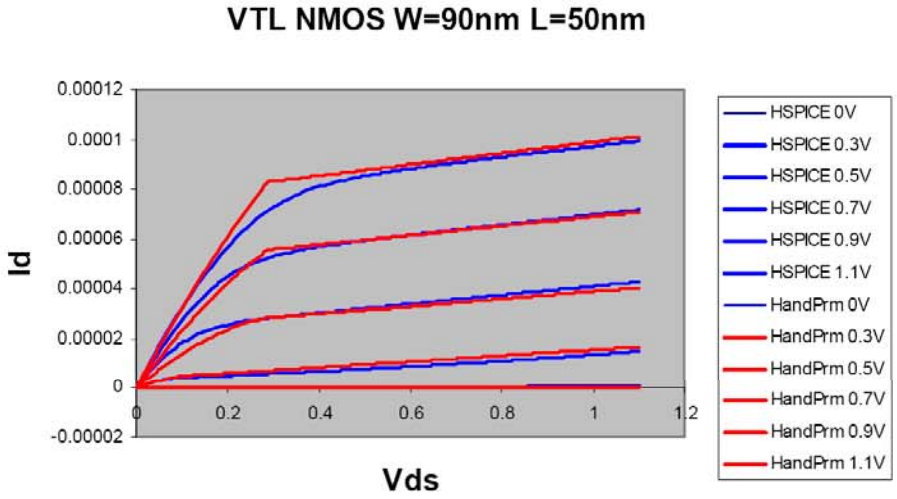
where $V_{\min} = \min(V_{GS} - V_T, V_{DS}, V_{DSAT})$

- channel resistance (r_{ch}) parameter added to more closely match our SPICE models

Model Improvement with r_{ch}

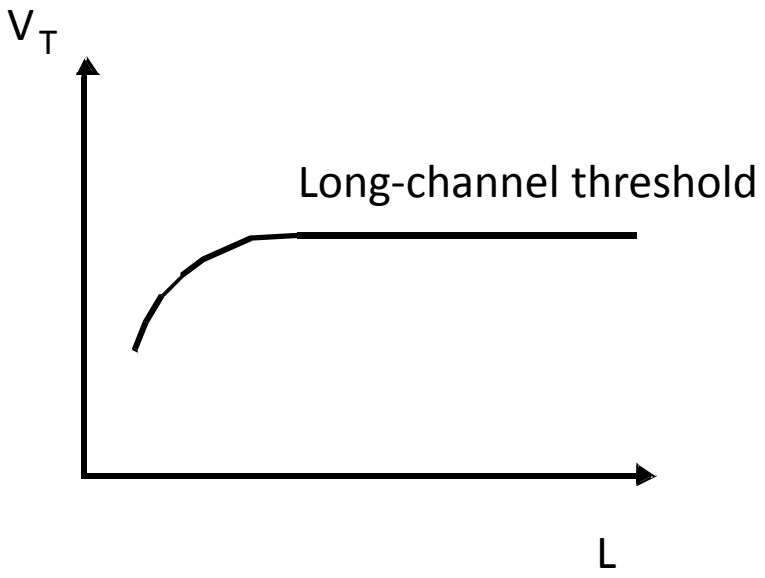


without r_{ch}

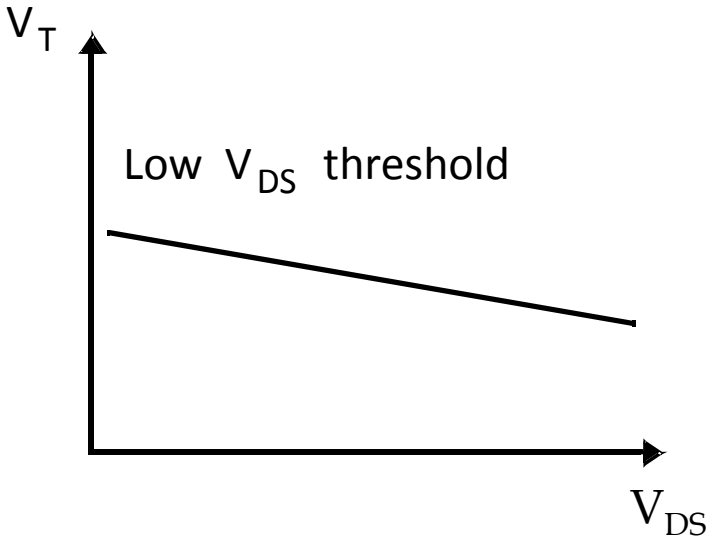


with r_{ch}
(Matches better for low values of Vgs)

Threshold Variations



Threshold as a function of the length (for low V_{DS})



Drain-induced barrier lowering (for low L)

Summary: Standard Equation

- Linear / Tridode Region:

$$I_D = k' \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^{\ 2}}{2}\right]$$

- Saturation Region:

$$I_D = \frac{k'}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda \quad V_{DS})$$

- Velocity Saturated Region:

$$I_D = \frac{1}{1 + \left(\frac{V_{DS}}{\xi_C L}\right)} k' \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^{\ 2}}{2}\right](1 + \lambda \quad V_{DS})$$

- Subthreshold Region:

$$I_D = I_S e^{\frac{V_{GS}}{nkT/q}}\left(1 - e^{-\frac{V_{DS}}{kT/q}}\right)$$

- Threshold Voltage:

$$V_T = V_{T0} + \gamma \quad \left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$$